Design of very low voltage CMOS rectifier circuits

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Abstract— **This paper presents a simple analytical model of the basic rectifier circuit for very low voltage operation based on the Shockley (exponential) law of the diode. The main alternatives for the implementation of diodes in CMOS technologies and the calculation of the equivalent diode parameters for low voltage operation are summarized. The model of the half-wave rectifier for very low voltage is verified with measurements on a circuit built with a 1N4148 diode. The main diode implementations using MOS transistors of a 0.13 µm technology operating in weak inversion are analyzed and a very simple design procedure is suggested.**

I. INTRODUCTION

The demand for rectifier circuits that can efficiently operate at very low voltages is increasing as a consequence of the growing interest for RFID tag chips [1]. Low-voltage rectifiers are also used to process energy harvested from vibrations [2] or even from the body movement [3]. The use of energy harvesting has also been considered for biomedical devices [3]. In many energy harvesting devices, a rectifier circuit generates the dc voltage from a received ac or rf voltage. Since in these applications the ac voltages are usually not larger than a few hundred milivolts, a voltage multiplier circuit (Fig. 1) is used to obtain a dc voltage of the order of 1V.

II. PREVIOUS WORK

In our previous work [2] we designed voltage multipliers using MOS transistors operating as diodes in the AMIS 0.5 µm and AMS 0.35µm technologies. Tests on the fabricated chips indicated requirements of minimum input voltage of 400m V_{peak} and 150 mV_{peak} for the chips in the AMIS 0.5µm and AMS0 0.35µm, respectively. Since there is no available analytical model for the rectifier operating at very low voltage, our previous designs were obtained after the simulation of many alternatives. The industrial need for a useful exploration of the available design space for low voltage rectifiers motivates the present work. Since the design of the voltage multiplier of Fig. 1 can be reduced to the design of the half wave rectifier of Fig. 2 [1] we will in the following focus on the performance of the topology of Fig. 2.

*This work was supported by CNPq – Brazil.

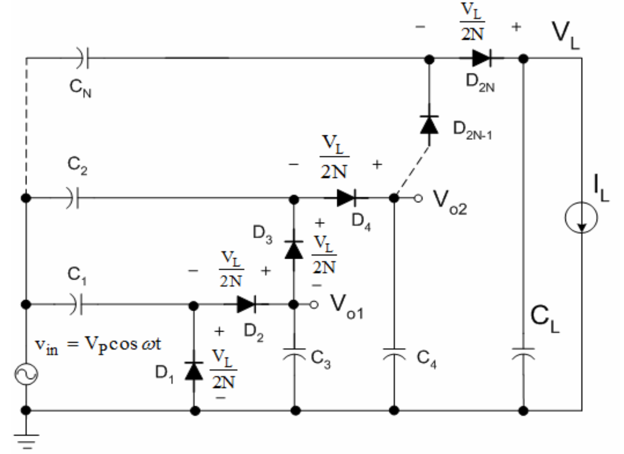


Fig.1 N-stage voltage multiplier.

III. HALF-WAVE RECTIFIER

Fig. 3 illustrates the steady-state operation of the half wave rectifier of Fig. 2 for an input peak voltage *Vp* of 600 mV.

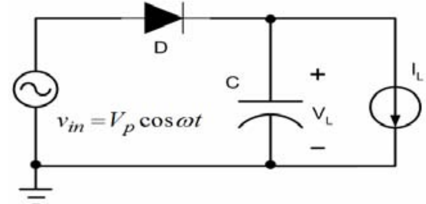


Fig. 2 Half-wave rectifier circuit with a dc current load.

In Fig. 3a the load voltage is nearly constant and, as a consequence, the peak diode current occurs simultaneously with the peak input voltage. In Fig. 3b and 3c, the ripple voltage ΔV and the phase difference between the peaks of input voltage and diode current $\Delta\phi$, which depend on the load current, are shown. For the low voltage operation illustrated in Fig. 3, a constant voltage drop model of the diode is clearly inappropriate, and we must use the Shockley (exponential) diode model:

$$i_D = I_S \cdot \left(e^{\frac{v_D}{n \cdot \phi_t}} - 1 \right) \quad (1)$$

$$v_D = V_P \cdot \cos(\omega \cdot t) - V_L \quad (2)$$

where I_S is the diode saturation current, ϕ_t is the thermal voltage, n is slope factor and V_L is the load voltage.

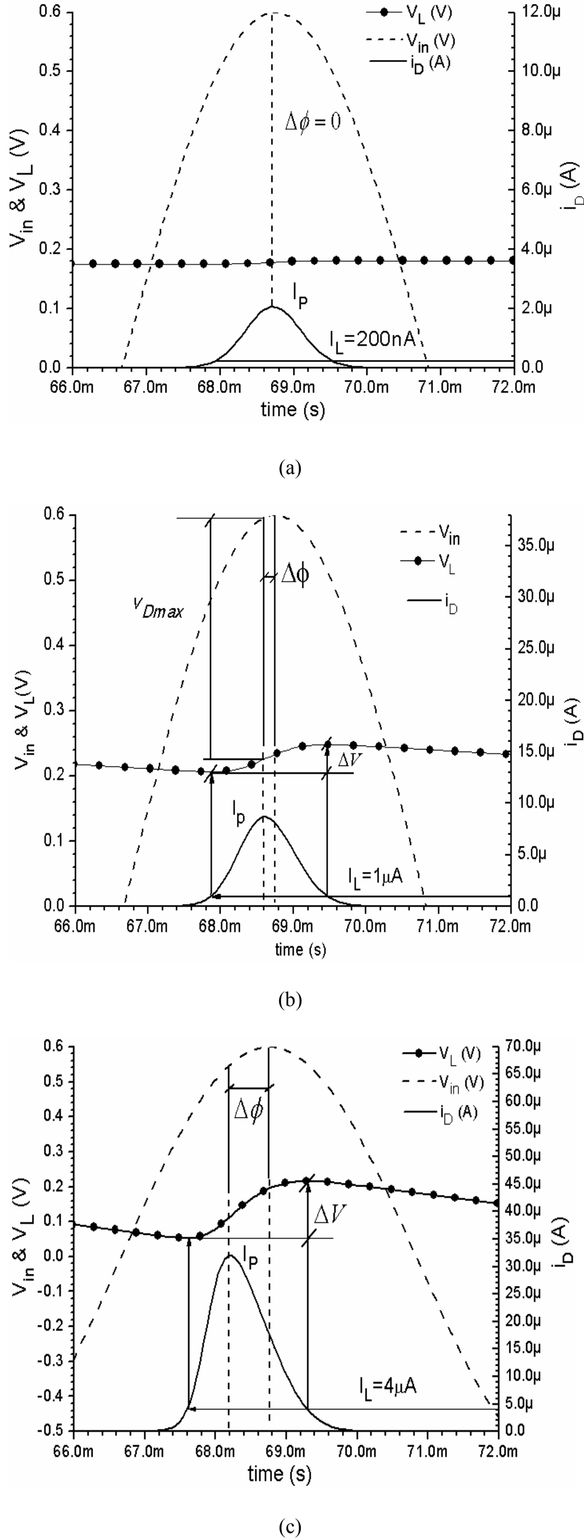


Fig. 3 Input and output voltage and diode current of the rectifier of Fig. 2 for (a) I_L= 200 nA, (b) I_L=1µA, (c) I_L=4µA.
The diode parameters are I_S = 4.4 nA and $n\phi_t$ =45 mV, C=150nF, f=120Hz, ΔVcalc. (fig.3b) = 46mV, ΔVcalc. (fig.3c) = 182mV .

To calculate the DC current I_L, we integrate (1) over one period.
The dc component of the diode current equals the load current I_L' thus using (1) and (2) we have

$$\frac{1}{T}\cdot\int_0^T i_D\cdot dt=\frac{1}{2\pi}\int_{-\pi}^{\pi} I_S e^{(V_P\cos\theta-V_L)/n\phi_t}d\theta-I_S=I_L \qquad (3)$$

Assuming that $V_P > n\ \phi_t$, the parabolic approximation of cosθ around zero and, consequently, the approximation of the diode current as a function of θ by the normal function are fair approximations as we will verify in the following. Thus, we approximate the diode current as

$$i_D\cong I_S\left(e^{(V_P-V_L)/n\phi_t}e^{-V_P\theta^2/2n\phi_t}-1\right) \qquad (4)$$

Assuming a well filtered output, V_L can be taken as constant, thus, the substitution of (4) into (3) leads to [4]

$$I_L\cong\frac{1}{2\pi}\int_{-\infty}^{+\infty} i_D d\theta=I_S\left(\sqrt{\frac{n\phi_t}{2\pi V_p}}e^{\frac{V_P-V_L}{n\phi_t}}-1\right) \qquad (5)$$

The analytical expression in (5) is equivalent to the use of the asymptotic expression below for the calculation of the zero order modified Bessel function $B_0(x)$ [5],

$$B_0(x)\cong\frac{e^x}{\sqrt{2\pi x}} \qquad (6)$$

$$x=\frac{V_P}{n\cdot\phi_t} \qquad (7)$$

For x > 3, the error in (6) is below 5% [5].
Finally, from (5) we calculate the dc load voltage as

$$V_L=V_P-n\phi_t\ln\left[\sqrt{\frac{2\cdot\pi\cdot V_P}{n\cdot\phi_t}}\left(1+\frac{I_L}{I_S}\right)\right] \qquad (8)$$

In (8), the second (logarithmic) term, which substitutes the constant V_{on} term of the conventional rectifier model, represents the maximum voltage drop on the diode.
The peak value of the diode current calculated from (4) and (8) is

$$I_P=I_S e^{\frac{V_P-V_L}{n\cdot\phi_t}}\cong I_L\sqrt{\frac{2\pi V_P}{n\phi_t}} \qquad (9)$$

Finally, defining the conduction angle of the diode as that for which the charge that flows through the diode is 95% of the total charge in a cycle (Fig. 4) and using the normal function approximation for the diode current (4), we find that

$$\theta_C=4\sigma=4\sqrt{\frac{n\phi_t}{V_P}} \qquad (10)$$

Thus, the conduction angle depends only on the V_P/ϕ_t ratio.
Once we have found the conduction angle, the voltage ripple ΔV, shown in Fig. 3b and 3c, can be calculated as

$$\Delta V\cong\frac{I_L T}{C}\left(1-\frac{\theta_C}{2\pi}\right) \qquad (11)$$

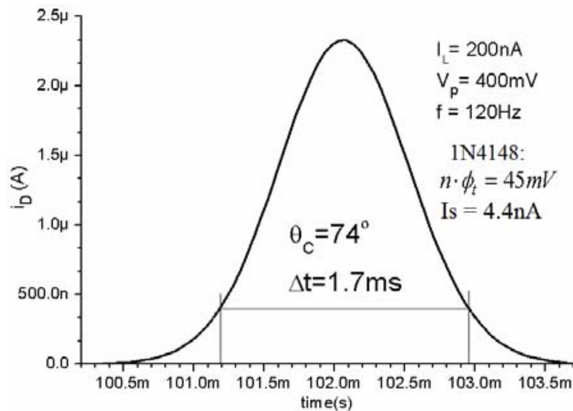


Fig.4. Simulated diode current that illustrates the definition of the conduction angle θ_C.

Results of measurements of the half-wave rectifier using a diode 1N4148 are shown in Figs. 5 - 7 and in Table I.

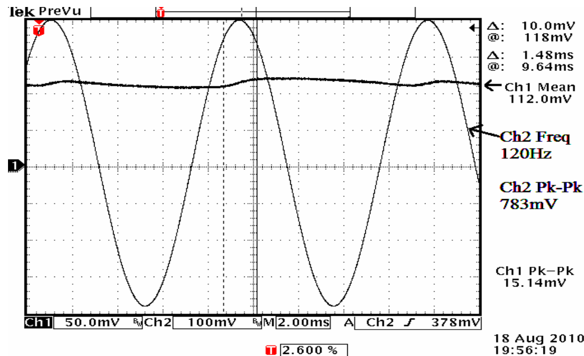


Fig. 5 Measured input and output waveforms on half-wave rectifier built with the 1N4148 diode. Vp=400mV I_L=200nA. C=150nF.

In Fig. 6 we can observe the fair fitting of eq. (8) for the ouput voltage of the rectifier with the 1N4148 diode for low values of the input voltage and for a wide range of output currents. Fig. 7 shows that the conduction angle is insensitive to load current. Finally, in Table I we summarize the comparison between experimental data and analytical model for I_L=200nA.

TABLE I

COMPARISON BETWEEN MEASUREMENTS AND CALCULATION ON THE HALF WAVE RECTIFIER FOR IL=200nA.

	Vp = 0.4V	Vp = 0.6V	Vp = 1.2V
VL calc. (8)	133mV	324mV	908mV
VL meas.	112mV	340mV	906mV
v_{DMAX} calc.(8)	266mV	276mV	291mV
v_{DMAX} meas.	284mV	310mV	311mV
Ip calc.(9)	1.6μA	1.9μA	2.6μA
Ip meas.	1.5μA	1.8μA	2.5μA
θc calc.(10)	77°	63°	44°
θc meas.	74°	65°	47°

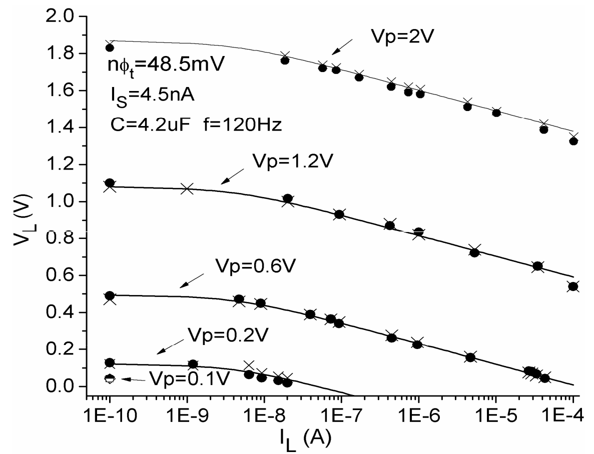


Fig. 6.Comparison between measured and calculated output voltage V_L of the half-wave rectifier vs. load current

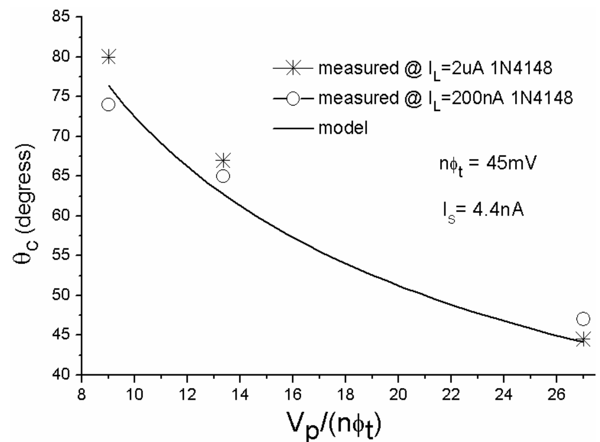


Fig. 7. Comparison between measured and calculated diode conduction angle of the half-wave rectifier vs. normalized input voltage.

IV. IMPLEMENTATION OF DIODES IN CMOS TECHNOLOGIES

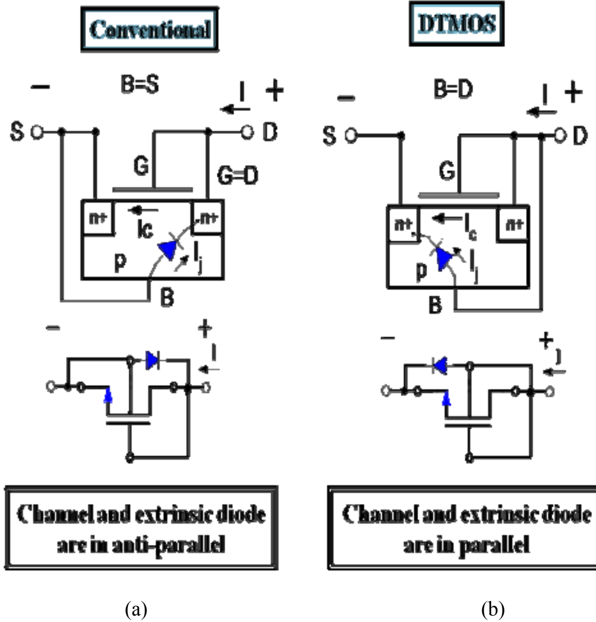
Figure 8 shows the two possible topologies for the MOS transistor connected as a diode. It is important to note that the diode current is composed by the channel current plus the current of the extrinsic diode. The disadvantage of the MOS transistor in the usual connection, with the bulk (B) tied to the source (S) (Fig. 8a), is the high reverse current. In effect, the reverse current of the device in Fig. 8a is due to the direct current in the extrinsic diode which increases exponentially with the increase of the magnitude of the reverse bias. To avoid the high reverse current of the conventional MOS diode, the DTMOS (Dynamic Threshold voltage MOSFET). connection can be used. In effect, in the DTMOS connection of the MOSFET, with the gate (G) tied to the substrate (Fig. 8b), the channel and the extrinsic diode are in parallel. The DTMOS connection can be used for p channel transistors in an n-well process or for the nMOS transistors in p- or triple-well processes. To model the MOS diodes, we will use, for the sake of simplicity, the weak inversion model, which is appropriate for low voltage operation.

The drain to source current is expressed [6] by:

$$I_{DS} = \frac{W}{L} I_o \, e^{\frac{V_{GB}-V_{TO}}{n \cdot \phi_t}} \left[e^{\frac{-V_{SB}}{\phi_t}} - e^{\frac{-V_{DB}}{\phi_t}} \right] \quad (12)$$

$$I_O = \mu_0 n C'_{ox} \phi_t^2 e^1 \quad (13)$$

where μ_0 is the carrier mobility, C'_{ox} the oxide capacitance per unit area, W/L the transistor aspect ratio, n the transistor slope factor and V_{TO} the threshold voltage.



(a) (b)

Fig. 8. The two possible connections of a MOS transistor as a diode.

For the DTMOS connection of Fig. 8b, we have from (12)

$$I_D = \frac{W}{L} I_o \cdot e^{\frac{-V_{TO}}{n \cdot \phi_t}} \left[e^{\frac{v}{\phi_t}} - 1 \right] \quad (14)$$

where $v = -V_{SB}$ and the saturation current I_S of the implemented diode is given by

$$I_S = \frac{W}{L} I_o \cdot e^{\frac{-V_{TO}}{n \cdot \phi_t}} \quad (15)$$

Since for the DMOS $V_{GB} = V_{DB} = 0$, the DTMOS diode behaves as an ideal diode with ideality factor $n = 1$ for low voltage (weak inversion) operation, as shown in (14). It is interesting to observe that the I_S current in (14) corresponds to the saturated drain current of the transistor with $V_{GS} = V_{SB} = 0$. As is clear from (15), to obtain a diode with high I_S saturation current, for efficient low voltage operation, we must use a technology with a low V_{TO} and design the adequate geometric factor W/L. Finally, the simulated characteristics of some of the diode structures available in a 0.13 µm technology are shown in Fig. 9.

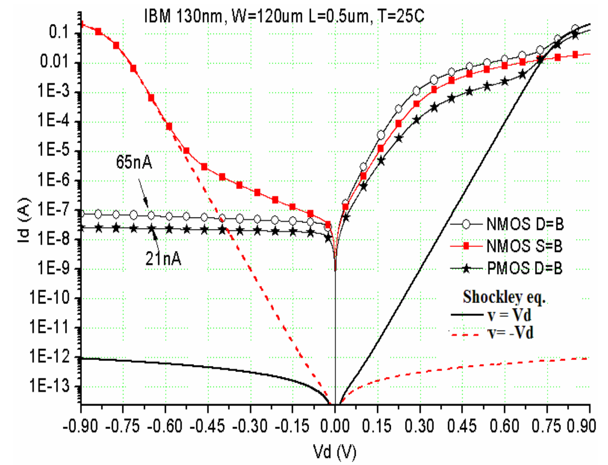


Fig 9 I-V characteristics for some diode connected transistors in a 0.13 µm technology Junction Diode: $n\phi_t$=37mV

V. SUMARY

A simple analytical model for the low voltage rectifier was presented. Equation (8) allows determining the minimum peak input voltage for a given diode and load requirements. Conversely, the knowledge of the input voltage allows determining the diode I-V characteristics for the load requirements. We have also shown that the conduction angle of the diode is independent of the load current. The analytical model, when used with data extracted from the simulated characteristics of MOSFET diodes, allows the rapid exploration of the design space of low voltage rectifiers in CMOS technologies. In its simplest form the design consists of the two following steps: first, determine I_S from the rectifier requirements using (8); second, calculate the transistor aspect ratio from (15).

REFERENCES

[1] J.-P. Curty, N. Joehl, F. Krummenacher, C. Dehollain and M. Declercq, “A model for µ-power rectifier analysis and design,” *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 52. no. 12, pp. 2771-2779, Dec. 2005.

[2] A. J. Cardoso, C. G. Montoro and M.C. Schneider. “CMOS Rectifier Design for Energy Harvesting based on Vibrations,” *XV Wokshop IBERCHIP*, Iguaçu Falls, Brazil, 2010, pp.241-245.

[3] R. Amirtharaj, P. Wright, “Energy Harvesting for Biomedical Devices and Health Care Intelligent Infrastructure”, available at http://www.citris-uc.org/research/projects/energy_harvesting_for_biomedical_devices_and_health_care_intelligent_infrastructure

[4] P. C. Dunn, *Gateways Into Electronics*. John Wiley and Sons, New York, 2000.

[5] M. Abramowitz and I. S. Stegun, *Handbook of Mathematical Functions*, Dover Publications, New York, 1970.

[6] E. Vittoz and J. Fellrath, “CMOS analog circuits based on weak inversion operation,” *IEEE J. Solid State Circuits*, vol. 12, no. 3, pp. 224-231, June 1977.